Listing of the Claims:

1 (previously presented): A clock and data recovery circuit (CDR) generating a recovery clock according to an input data and a reference clock corresponding to the input data, the CDR comprising:

a phase shifter generating M discrete clocks at different phases according to the reference clock;

a data sampler generating a select signal according to the input data and the M discrete clocks;

a primary phase selector outputting two consecutive discrete clocks and at least one interpolated clock with a phase between the phases of the two consecutive discrete clocks, according to the select signal, wherein the two consecutive discrete clocks and the interpolated clock have approximately the same frequency as the reference clock and the input data;

a multiplexer selecting one of the two consecutive discrete clocks or the interpolated clock to be a selected output clock;

a phase detector receiving the selected output clock to be the recovery clock, and outputting an advanced calibration signal if the recovery clock leads or lags the input data;

an advanced phase selector receiving the advanced calibration signal, and transmitting the phase select signal to the multiplexer for adjusting the selection of the selected clock, and a primary calibration signal to the primary phase selector for adjusting the two consecutive discrete clocks and at least one corresponding interpolated clock.

2 (original): The CDR of claim 1, wherein the phase shifter is an analog phase-locked loop (APLL).

3 (original): The CDR of claim 1, wherein the phase shifter is a delay-locked loop (DLL).

4 (original): The CDR of claim 1, wherein the data sampler comprises M edge-triggered flip-flops, the input data is input to clock input ends of the M edge-triggered flip-flops, and the M discrete clocks are input to data input ends of the M edge-triggered flip-flops, respectively.

5 (original): The CDR of claim 4, wherein the edge-triggered flip-flops are D flip-flops.

6 (original): The CDR of claim 1, wherein the recovery clocks can be used to trigger the input data in order to generate a recovery data.

7 (original): The CDR of claim 1, further comprising a counter connected between the data sampler and the phase detector for ensuring the stability of the input data and then inputting the input data to the data sampler.

8 (original): The CDR of claim 1, wherein when the recovery clock lags the input data, the advanced calibration signal is output as plus 1, and when the recovery clock leads the input data, the advanced calibration signal is output as minus 1.

9 (original): The CDR of claim 8, wherein the phase select signal of the advanced phase selector is modified according to the advanced calibration signal; and when both the two consecutive discrete clocks and the interpolated clock selected by the multiplexer according to the phase select signal lag or lead the input data, the advanced phase selector outputs the primary calibration signal.

10 (original): The CDR of claim 8, wherein the primary phase selector is comprised of a plurality of inverters, and at least one interpolated clock can be formed by the two consecutive discrete clocks using inverters having different width/length

(W/L) proportions.